ABSTRACT OF THE DISCLOSURE

A signal-processing circuit in which two-stage equalization is carried out by using first and second equalization circuits provided on the upstream and downstream sides from a phase locked loop circuit, respectively, is provided, wherein the first equalization circuit on the upstream side from the phase locked loop circuit is composed of a transversal filter, to minimize an equalization error caused by the first equalization circuit, thereby stabilizing the operation of the phase locked loop circuit. Another signal-processing circuit including an analog-to-digital converter and a digital phase locked loop circuit for receiving the output from the analog-to-digital converter, and a recording and playback apparatus using the same are also provided, wherein the output from the analog-to-digital converter is input as the digital signal in the digital phase locked loop circuit, to fetch a detection point voltage, thereby stabilizing the operation of the phase locked loop circuit without the need of provision of any analog circuit.